UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/943,209	08/29/2001	William K. Lam	0007056-0186/P5729/KO	8850

32615 7590 09/03/2004

OSHA & MAY L.L.P./SUN
1221 MCKINNEY, SUITE 2800
HOUSTON, TX 77010

EXAMINER	
VU, TUAN A	

ART UNIT	PAPER NUMBER
2124	

DATE MAILED: 09/03/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/943,209	LAM ET AL.	
	Examiner	Art Unit	
	Tuan A Vu	2124	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 August 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-8* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *29 August 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☒ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This action is responsive to the application filed August 29, 2001.

Priority papers (12/27/2001) have been acknowledged and accepted on record. Claims 1-8 have been submitted for examination.

Oath/Declaration

2. The declaration filed on 12/27/2001 has been put on record but contains the following informality.

> *It does not state that the person making the oath or declaration acknowledges the duty to disclose to the Office all information known to the person to be material to patentability as defined in 37 CFR 1.56.*

As stated in 37 CFR § 1.63, the Applicant must disclose information material to patentability under 37 C.F.R. 1.56, not a subset of 37 C.F.R. 1.56 (e.g. 1.56(a) - see para "We hereby claim the benefit ... of the application: " of instant declaration). Applicant is kindly asked to refer to 37 C.F.R. § 1.63 of the current MPEP, which now states that "... the person making the oath or declaration acknowledges the duty to disclose to the Office all information known to the person to be material to patentability as defined in § 1.56.", and apply the right form accordingly. A new oath or declaration in compliance with 37 CFR 1.67(a) identifying this application by application number and filing date is gently asked to be re-submitted. See MPEP §§ 602.01 and 602.02.

Claims objections

3. Claim 5 is objected to because of the following informalities: there no reciting of 'the trimming step'(line 1 of claim 5) in the base claim and Examiner will interpret this element as a processing step of claim 4 to examine the merits of the claims. Further, there is no reciting of

any 'minimal module' (line 2 of claim 5) in the base claim, hence this element is treated as the submodule. Appropriate correction is required.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1-8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Janniro et al., USPN: 5,634,098 (hereinafter Janniro), in view of Zambelich, "Totally Data-driven Automated Testing", copyright 1998, White Paper, *<http://www.dkl.com/pdf/datadriven.pdf>* or *<http://www.sqa-test.com/w_paper1.html>* (hereinafter Zambelich – slides document used herein).

As per claim 1, Janniro discloses a method of debugging software comprising:

obtaining a software target file (e.g source code *216, 222, 228, 234* – Fig. 2);

obtaining a first input test vector (step *406*, *412*, environment configuration file – Fig. 4);

obtaining a bug list (e.g. test list 810 – Fig. 8);

generating a first output vector (e.g. list *804* – Fig. 8) by applying said first input test vector to said target file;

applying a comparison test to said first output vector to determine whether a bug exists in said module (step 610 – Fig. 6).

But Janniro does not explicitly disclose that a source file in each directory in the hierarchy of directories (Fig. 2, 5) is a module; however, Janniro discloses the concept of

modularizing a test scheme and testing a block of source code and applying input and output matching thereto (Fig. 6). The concept of modularize a software testing process was a known concept in the art of software testing at the time the invention was made. Zambelich, in a method to automate test vectors or test cases similar to the generation of test configuration file by Janniro, discloses decomposing the test into test script applied to function and sub-routine level (e.g. slides 9-13); hence the concept of modular decomposition is suggested. Hence, it would have been obvious for one of ordinary skill in the art at the time the invention was made to modularize the hierarchized source files of Janniro so to apply the input vectors per blocks or modules as suggested by Zambelich because this approach would provide better error handling, maintainable result facilitating verification, and/or allow combinatorial testing, updatability on a per-test-script case basis and reduced redundancy of human intervention (see slide 13).

Nor does Janniro disclose applying a module decomposition test to said software module when the result of said comparison test is positive; and appending said software module and said first input test vector to said bug list when the decomposition test result is negative. The result of target code decomposition as suggested by Janniro being compared until there is no more blocks (see Janniro, Fig. 6) strongly suggests appending said block or a decomposed module portion to a bug list (i.e. software module and said first input test vector to said bug list) when there is no more possibility to decompose further, i.e. decomposition test result being negative. But Janniro does not explicitly disclose applying a module decomposition test to said software module when the result of said comparison test is positive. In view of the attempt to ensure that all the sub-routine are tested and that all the subdivisions of a target code is tested as suggested by both Janniro and Zambelich, it would have been obvious for one of ordinary skill in the art at the time

the invention was made to further the step of modularizing as taught by Zambelich's function/sub-routine decomposition and testing, e.g. when the test result of a higher level of code hierarchy is a success as suggested in Janniro's pushing the hierarchized blocks testing (step 616, Fig. 6) to more lower sub-levels because the more subdivided and tested the target software code is the better all the benefits thus set forth by Zambelich from above (slide 13) would stand out.

As per claim 2, Janniro discloses obtaining a predetermined output result vector and comparing first output vector to said predetermined output vector and determine whether said first output is at variance with said predetermined output result vector (e.g. col. 6, lines 32-49; step *610* – Fig. 6 – Note: the fact of comparing inherently teaches whether or not actual output deviates or how far it does from a standard median of the expected result, i.e. whether within acceptable variance margin); but does not explicitly disclose an optimal output result vector. Official notice is taken that the recording of an optimal result as a result from iterating from a plurality of tests being applied on a target object in order to obtain the least deviated and significant figures for further analysis or legacy referencing was a known concept in the art of software testing at the time the invention was made. Thus, it would have been obvious for one of ordinary skill in the art at the time the invention was made to implement the storing of the predetermined output vector as taught by Janniro so that such recorded output vector is a result optimized or averaged out value, i.e. optimal output vector, obtained from previous test output values being tallied on a specific target module, because persisting of the optimal value garnered from a plurality of test values would enable the most averaged out value to represent the output vector pertaining to different instances of test vectors or cases; thereby averting possible wide divergence in output values that would not fit to for persistence and/or further referencing.

As per claim 3, Janniro does not disclose obtaining a module decomposition list comprsing 2 or more submodules when the result of said decomposition test is positive; and iteratively processing said decomposition list. But in view of the pushing of the decomposition as suggested by the combination of Janniro and Zambelich being obvious from above, these limitations would also have been obvious because they fall under the same ambit and entails the same purposes leading to the same benefits as set forth above.

As per claim 4, Janniro disclose hierarchizing the input vectors according to a parent child tree configuration (e.g. col. 3, lines 23-42), hence suggesting for each subnodes in a tree a particular subset of input vectors is imparted thereto. Thus, the limitations as to obtaining a second input test vector, apply it to said sub-module for generating a second output vector; then recursively processing said submodule and second output test vector would also have been obvious in view of Janniro's above suggestion and the rationale as set forth in claims 1, 3 from above.

As in claim 5, the attempt to further decompose the software target module so as to address all the block or sub-routines has been addressed above in claim 1 and 3; hence the limitations as to obtaining the submodule and a first input test vector and apply this to the former would also have been obvious in view of the teachings by Janniro in claim 1 combined with Zambelich because for each further decomposed sub-routine or module, apply a appropriate set of input vector as suggested by the parent-child hierarchy of input vectors by Janniro (see col. 3, lines 23-42).

As per claim 6, Janniro discloses appending input test vector to a test list when the comparison test is positive (e.g. col. 18, lines 58-67); and recreating a bug when the comparison

test is negative, i.e. a first input vector being reapplied to generate a third output vector (e.g. col. 18, line 58 to col. 19, line 21)

As per claim 7, this step is an obvious variance of claim 3 (i.e. further decomposition and further lower level input vector with recursive applying of one to the other), therefore is rejected with the same corresponding rationale as set forth therein in view of the teachings to recreate the error as put forth in claim 6.

As per claim 8, Janniro discloses iterating more tests combining more input vectors and generating results in test list for recreating failed test and for storing successful test in specific order (re claim 6); and in view of the combined teachings by Janniro and Zambelich for furthering the decomposition so as to evidence more results from such decomposition as set forth from above, the limitation as to iterate from decomposition and reapplying specific sub-levels of input vectors to generate new output vectors would also have been obvious as set forth from above.

Conclusion

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tuan A Vu whose telephone number is (703)305-7207. The examiner can normally be reached on 8AM-4:30PM/Mon-Fri.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kakali Chaki can be reached on (703)305-9662.

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks

Washington, D.C. 20231

or faxed to:

(703) 872-9306 (for formal communications intended for entry)

or: (703) 746-8734 (for informal or draft communications, please label "PROPOSED" or "DRAFT" – please consult Examiner before use)

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington. VA. , 22202. 4th Floor(Receptionist).

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3900.

VAT
August 23, 2004

KAKALI CHAKI
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100